

The diagram shows the output OUT (pink) and inputs INPA (orange), INPB (green), INPC (red), INPD (purple), and INPE (brown) over 14 clock ticks. The output OUT is high when any of the inputs INPA through INPE are high. The FUNC signal is high from tick 1 to 14.

Signal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
FUNC	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INPA	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
INPB	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
INPC	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
INPD	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
INPE	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
OUT	0	1	1	1	1	1	0	0	0	0	0	1	1	0	0

OUT

Timestamp (125MHz FPGA clock ticks)